

Fig. 1

70317807 457782560

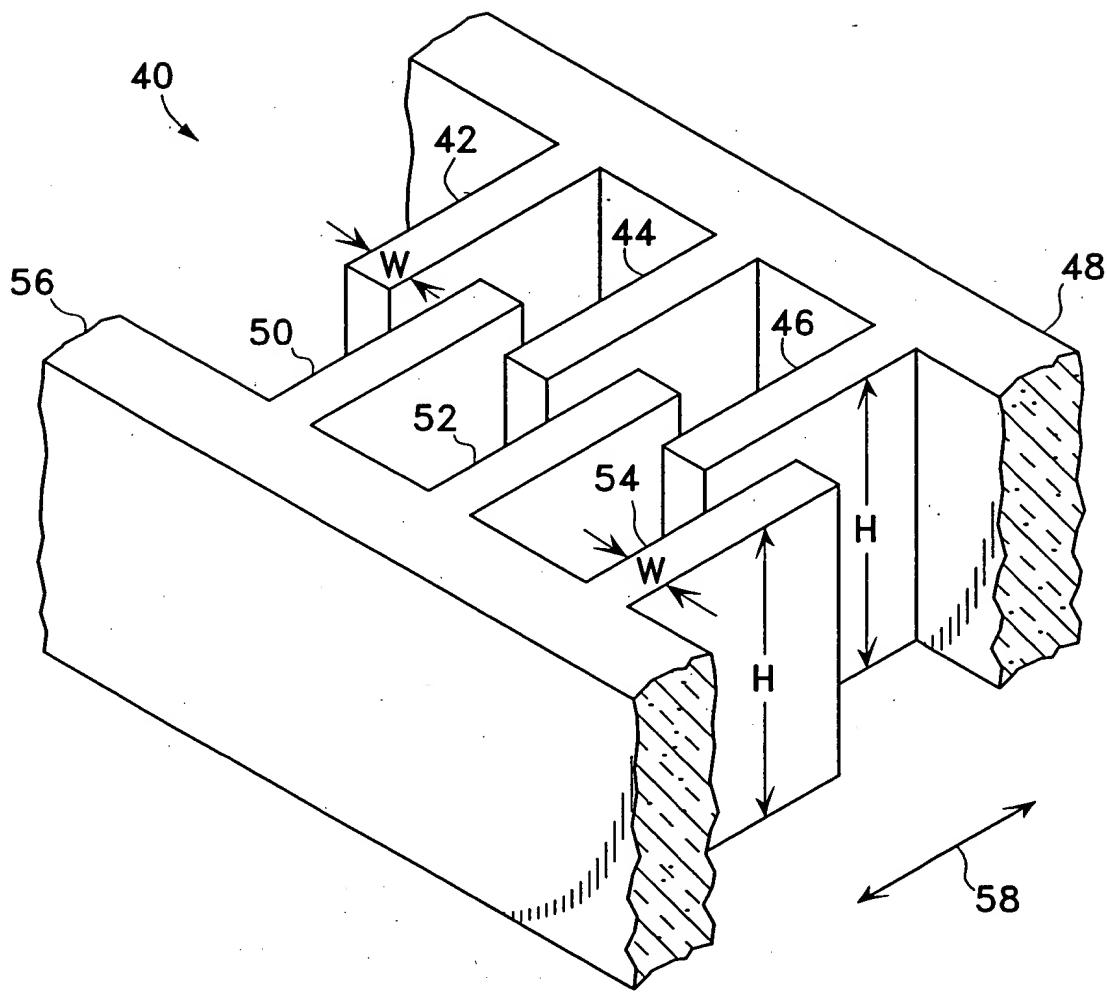


Fig. 2

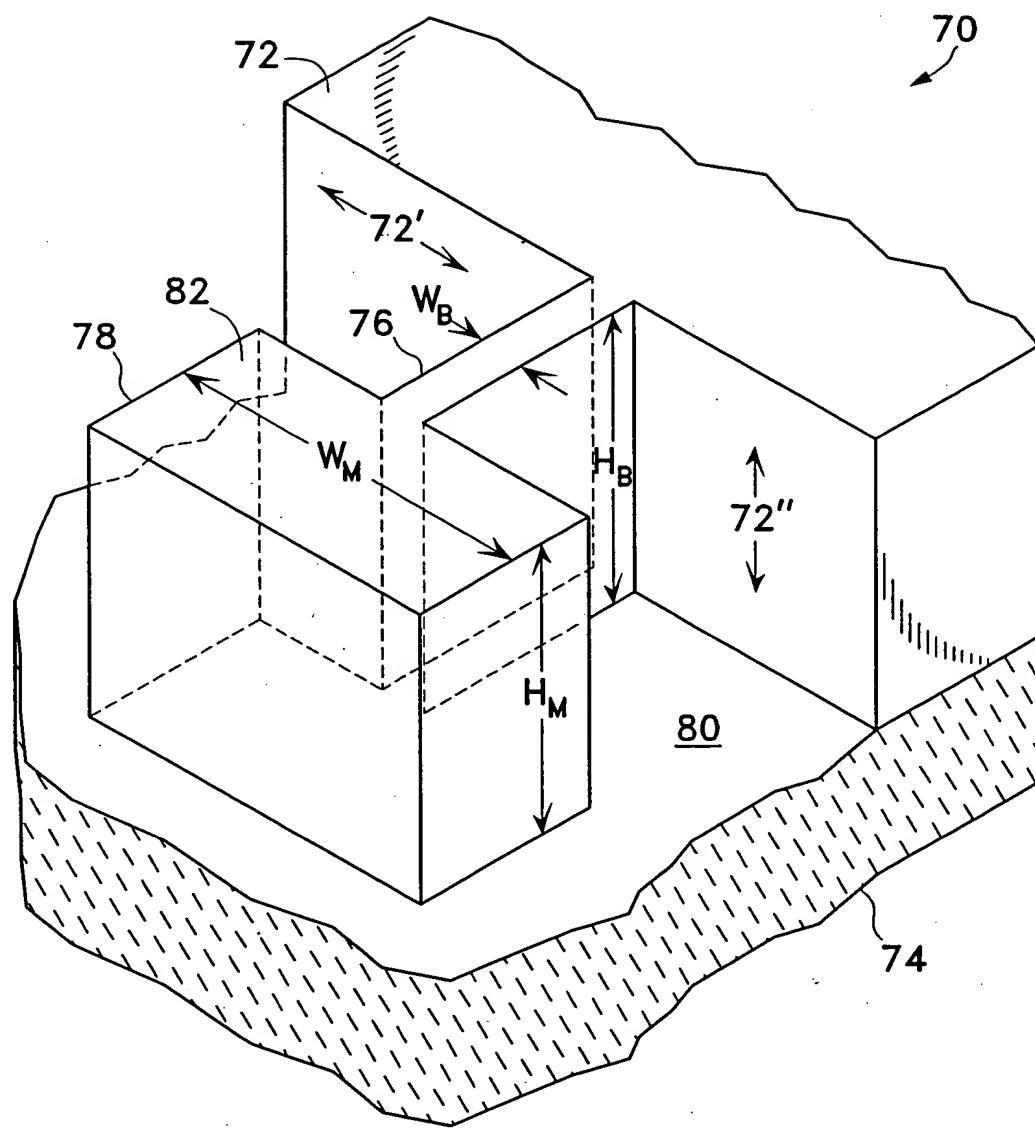


Fig. 3

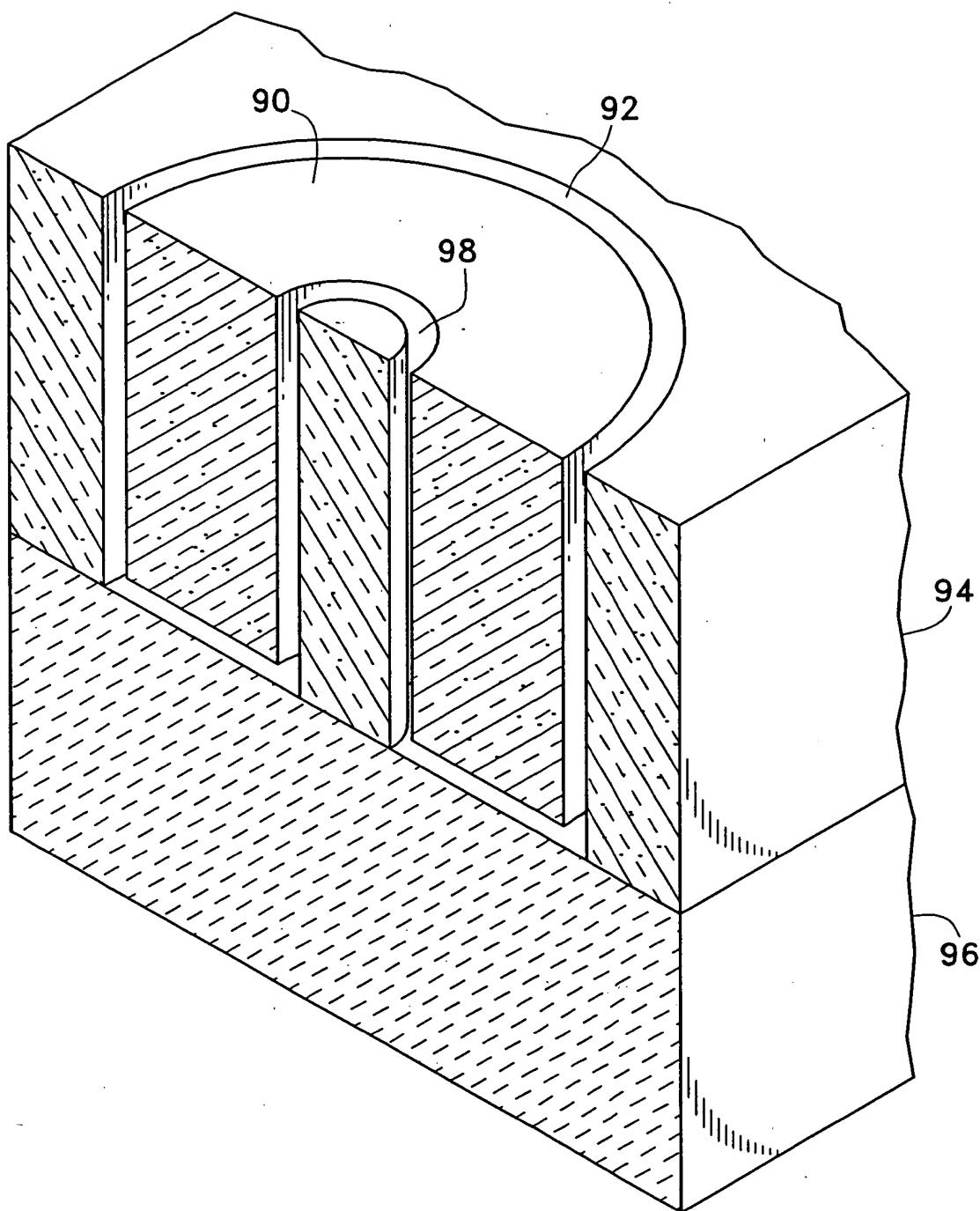


Fig. 4

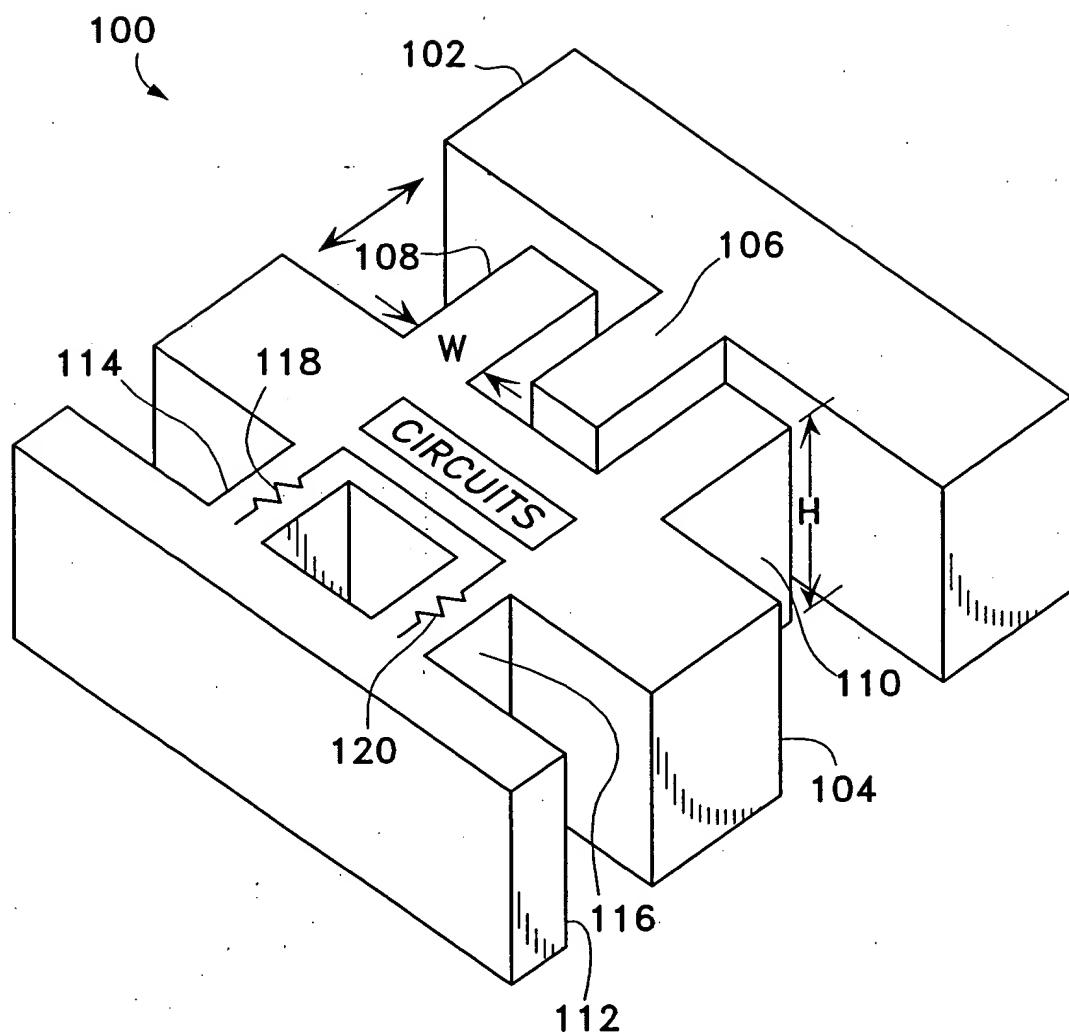


Fig. 5

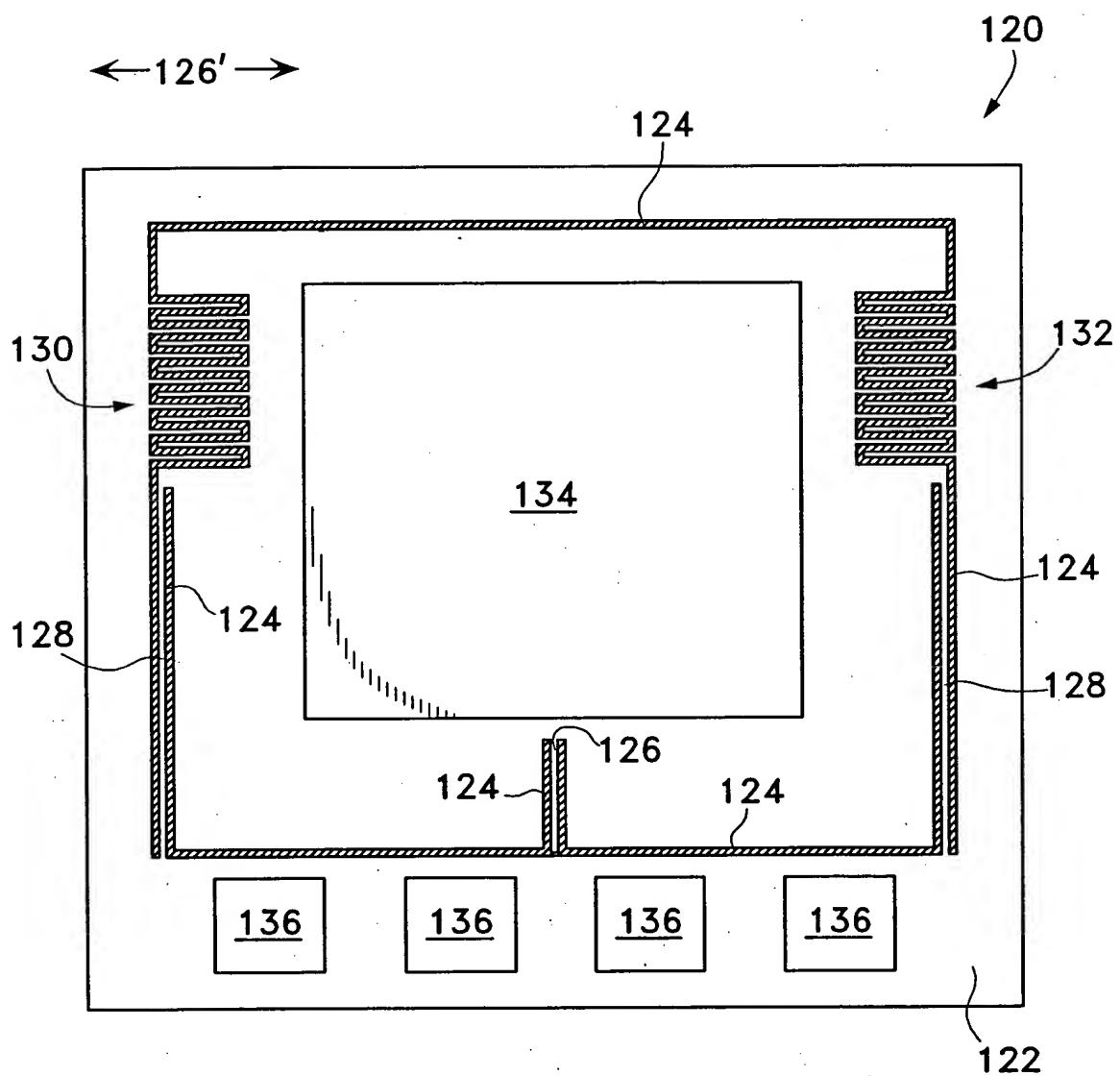


Fig. 6

100-130 = 115 7 8 2 6 5 0

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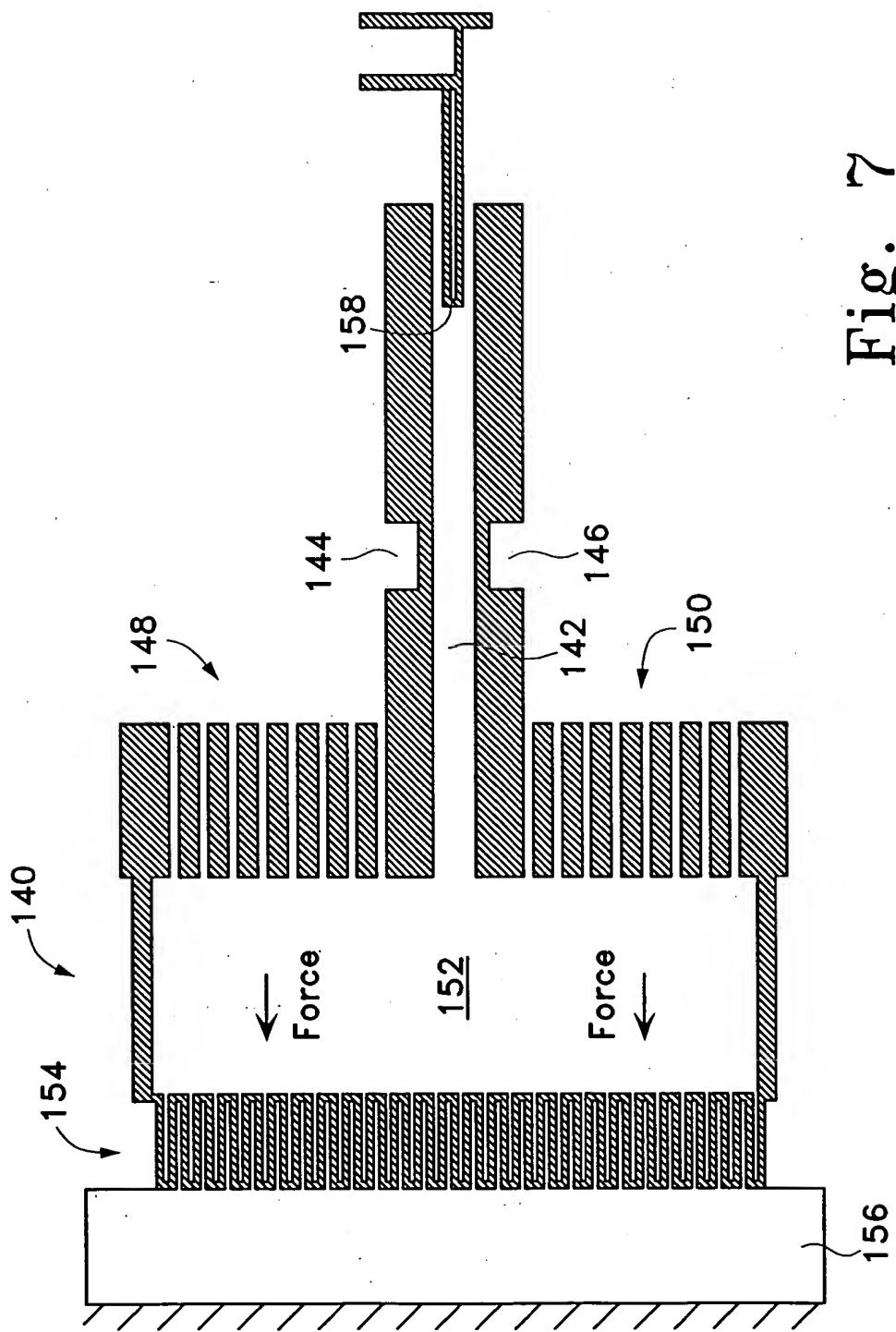


Fig. 7

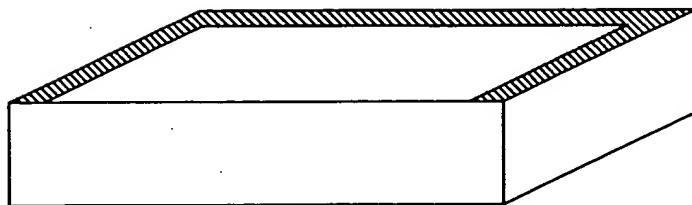


Fig. 8A

Pattern frontside with cavity mask  
and backside with alignment  
markers.

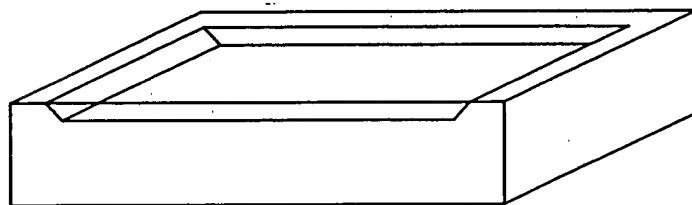


Fig. 8B

Timed anisotropic or plasma etch  
to form cavities.  
Strip frontside insulator.

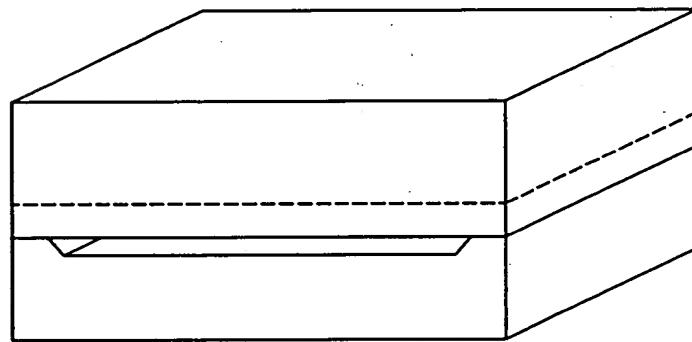


Fig. 8C

Silicon fusion band epi wafer to  
frontside. Epi thickness determines  
MEMS device thickness.

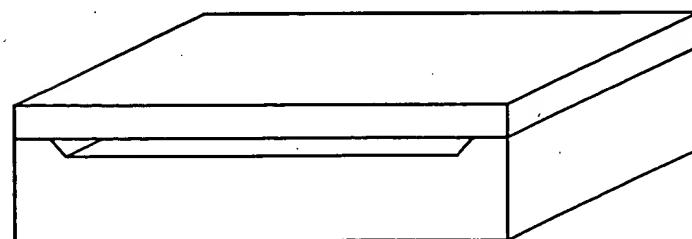


Fig. 8D

ECE etch to epi interface.

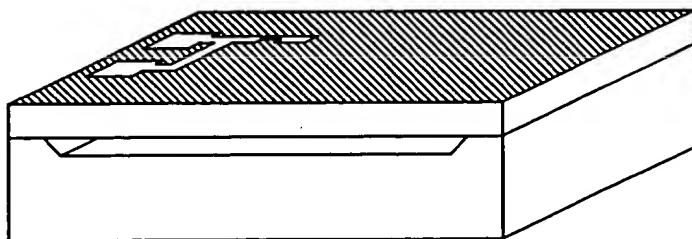


Fig. 8E

Deposit insulator on frontside and process sensing on chip circuits.

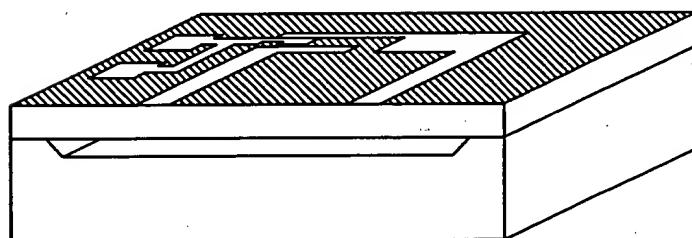


Fig. 8F

Define MEMS structure in insulator layer.

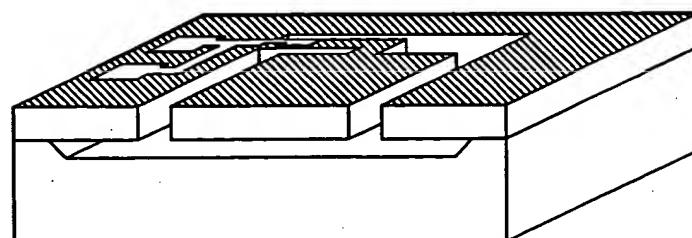


Fig. 8G

Anisotropic plasma etch to form MEMS structure.

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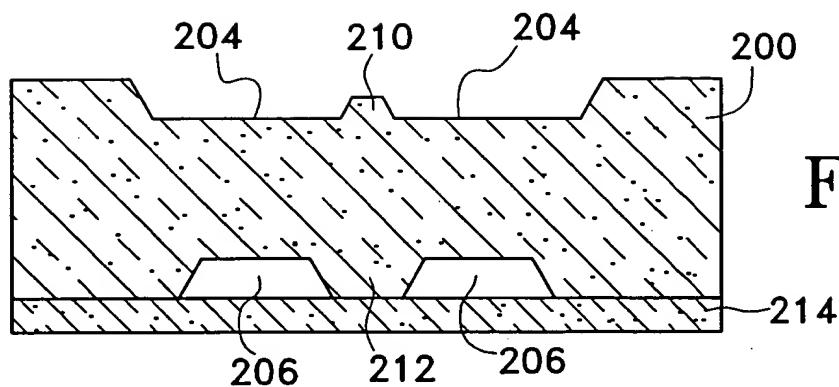


Fig. 9A

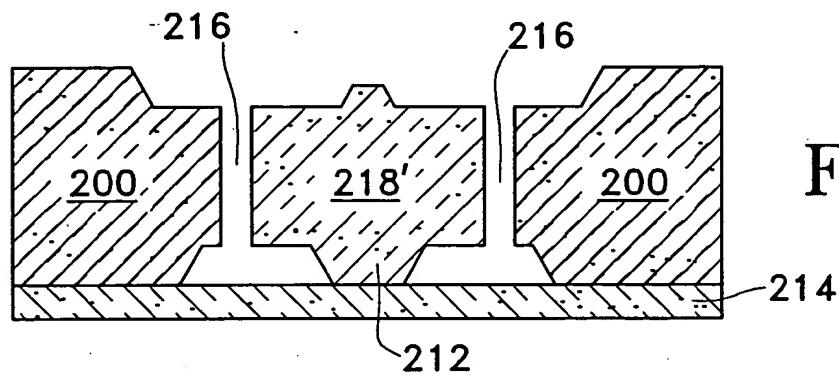


Fig. 9B

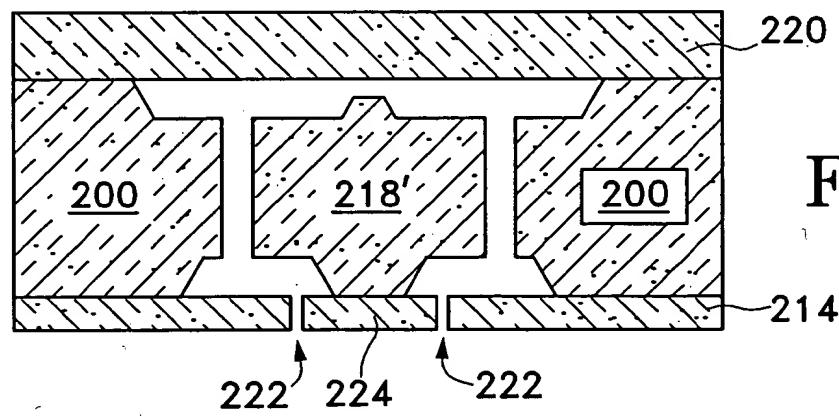


Fig. 9C

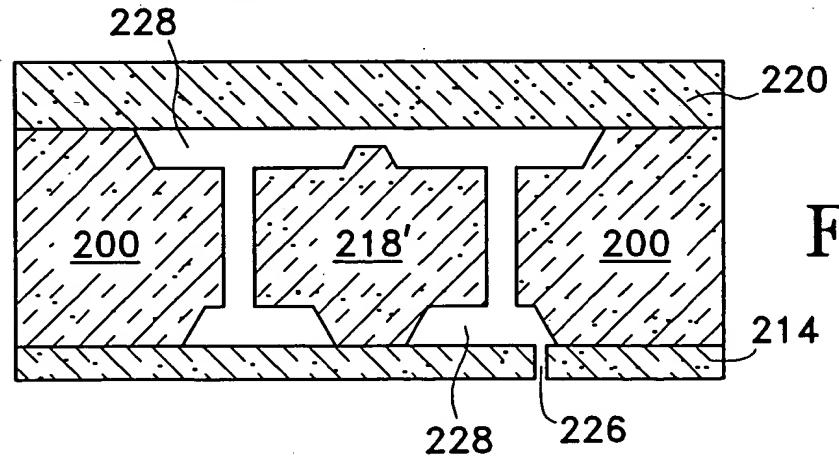


Fig. 9D

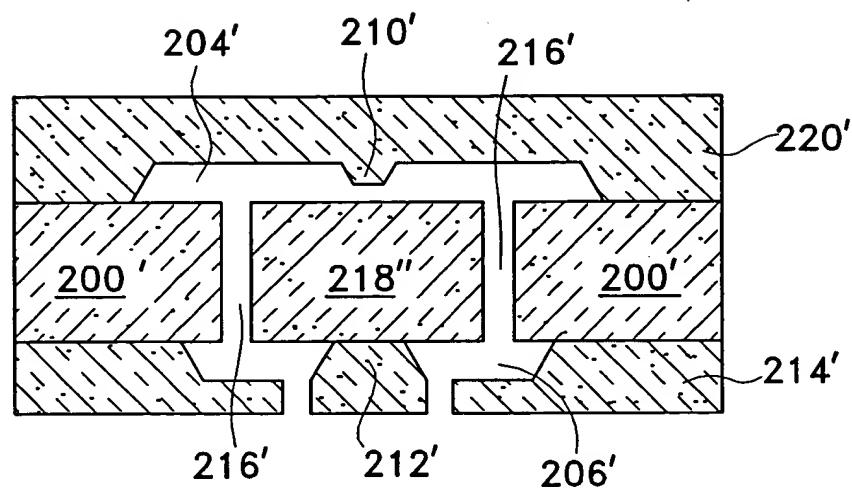


Fig. 10

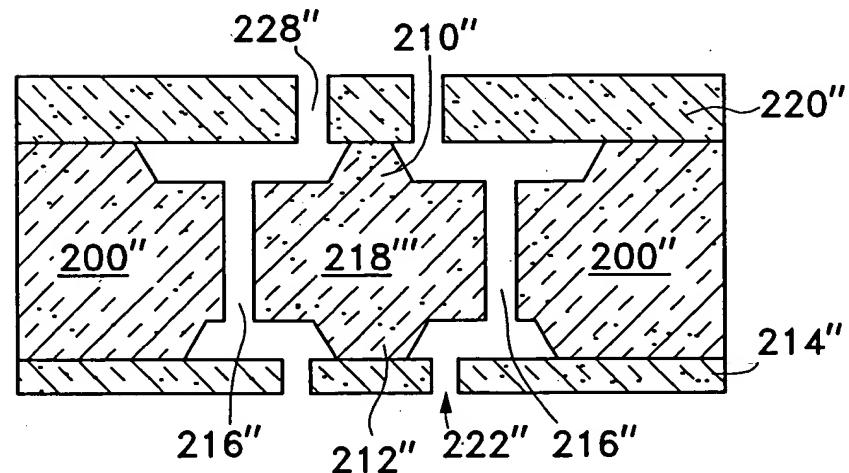


Fig. 11

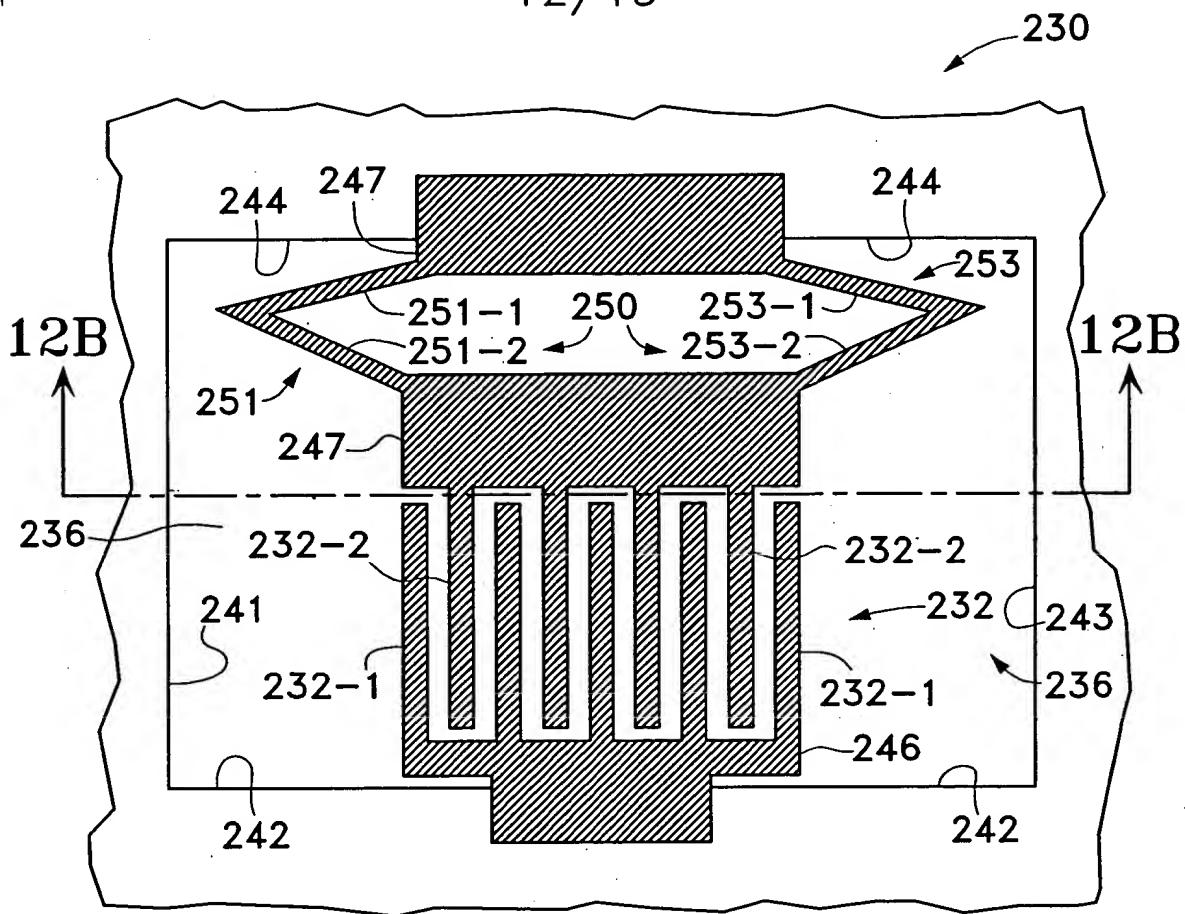


Fig. 12A

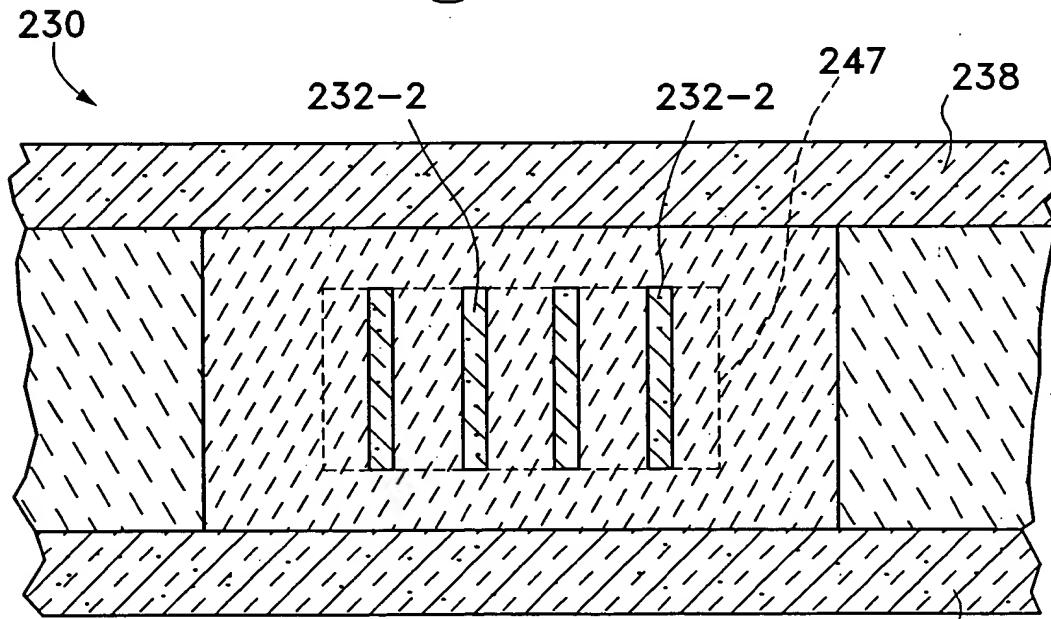


Fig. 12B

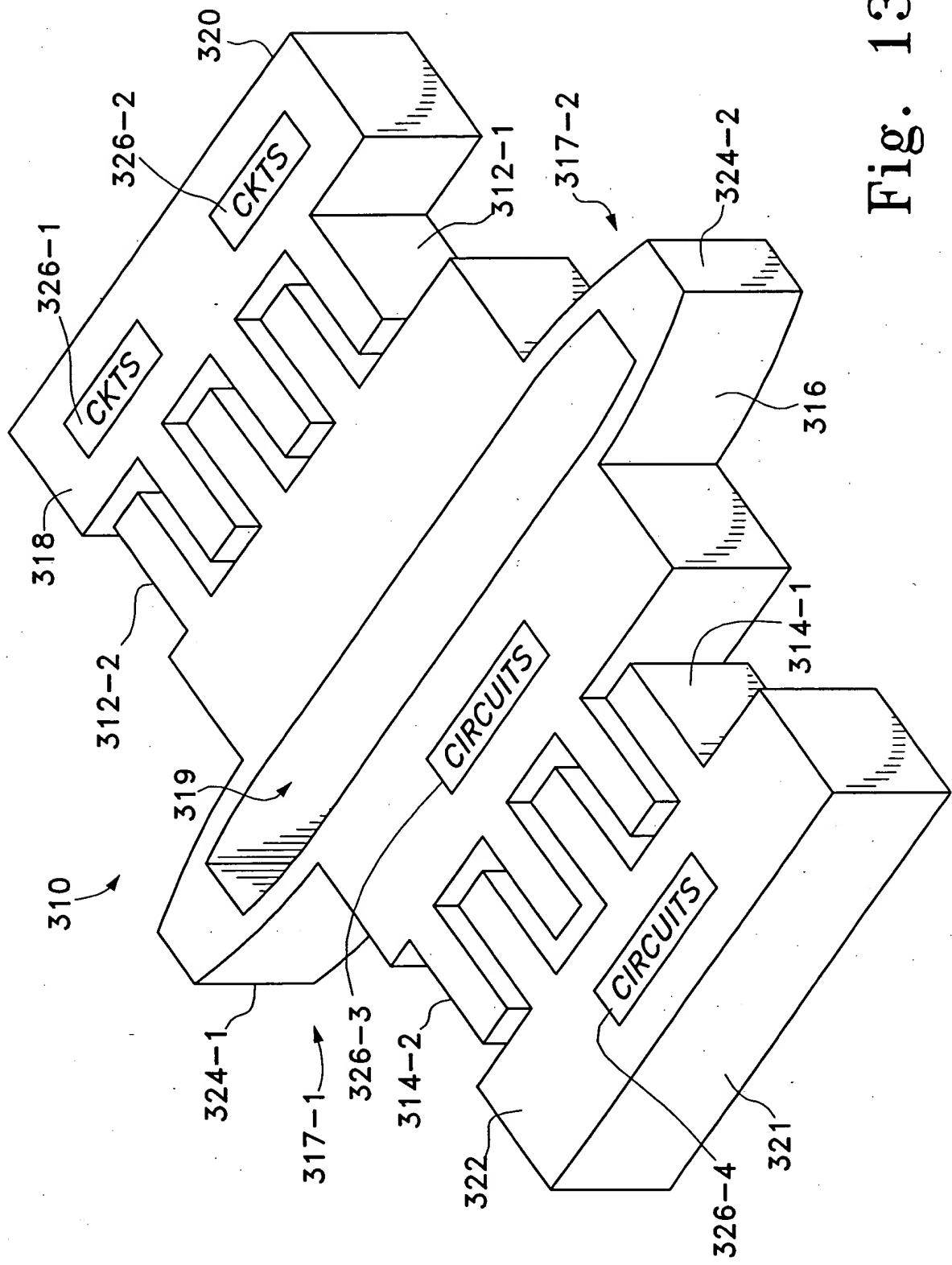


Fig. 13